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CmpE 124 Lab 4: Bipolar Circuits

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*Abstract*— The goal in this lab is to understand the electrical characteristics of bipolar circuits as well as understand the relationship between the output voltage of a CMOS device's propagation delay and its load.

# INTRODUCTION

The purpose of this lab is to build various circuits dealing with both npn transistors and CMOS devices. Using an oscilloscope, rise and fall times of the output voltage as well as propagation delays are measured to understand how they change as the CMOS device's load changes.

# Design methodology

## Parts List

* Breadboard
* 2N3904 npn transistor
* CD4069 CMOS inverters
* CD4011 2-input NAND gates
* CD4001 2-input NOR gates
* Tektronix AFG3021B Function Generator
* Tektronix DPO3032 Oscilloscope
* BNC to IC Hooks Cable
* Oscilloscope Probe

## Original and Derived Equations

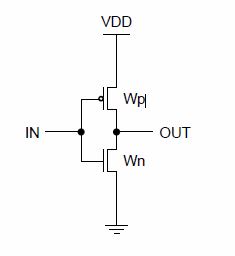
In order to calculate Rb and Rc for the npn transistor , the equations used were:

where Rc is the resistor at the transistor's collecter, Vcc is the source voltage, VCESAT is the voltage drop from the collector to the emitter during saturation, ICESAT is the current from the collector to the emitter during saturation, Rb is the resistor at the transistor's base, Vin is the input voltage signal, VBE is the voltage drop from the base to the emitter and IBSAT is the current flowing into the transistor's base.

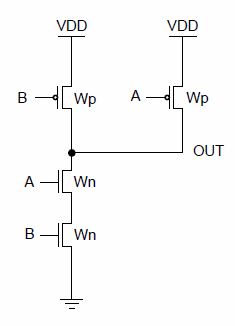
Schematic 4: CMOS NOR gate used in this lab.

## C:\Users\Kevin\Dropbox\schematic 1.JPGSchematics

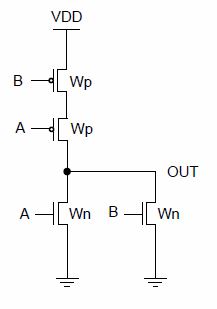
Schematic 1: The bipolar circuit design used to analyze an npn transistor.



Schematic 2: CMOS inverter used in this lab.



Schematic 3: CMOS NAND gate used in this lab.



# testing procedures

The testing procedure should be broken down into steps:

1. Step one.
2. Step two.

# testing results

In order to fit the constraints of the lab for the bipolar circuit where VBE is approximately 0.8 V and VCE is approximately 0.2 V, estimates have to be made for Rb and Rc. In order for the transistor to be saturated, Ibsat >> Icsat /β. After choosing Ic to be 40 mA, the resistor value for RC was calculated to be 120 Ω through Equation 1. Choosing Ib to be 1 mA to fit the saturation constraint, Rb was calculated to be 4.2 kΩ using Equation 2. Building the circuit shown in Schematic 1 with these calculated resistor values, VBE was measured at 0.817 V, IC was measured at 48 mA, VCE was measured to be 0.183 V, and Ib was measured to be around 1.10 mA. These measured values for VBE and VCE are close to the expected values of 0.8 V and 0.2 V respectively. The test results can be seen in figures 9 through 11.

# Conclusion

This was a very straight forward lab where the actual data aligned fairly well with the theoretical values. We did not have any issues during setup or testing.

# Appendices

(See attached pages)

# C:\Users\Kevin\Dropbox\Lab\lab4\data-raw\tek00000.pngappendices and references

Fig. 1a: Rise time of the output voltage of an inverter with no load.

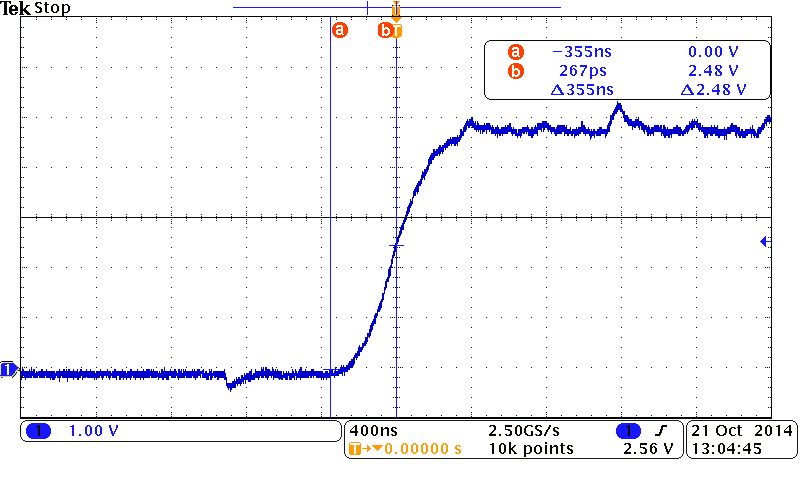


Fig. 1b: The rise time propagation delay of the output voltage of an inverter with no load

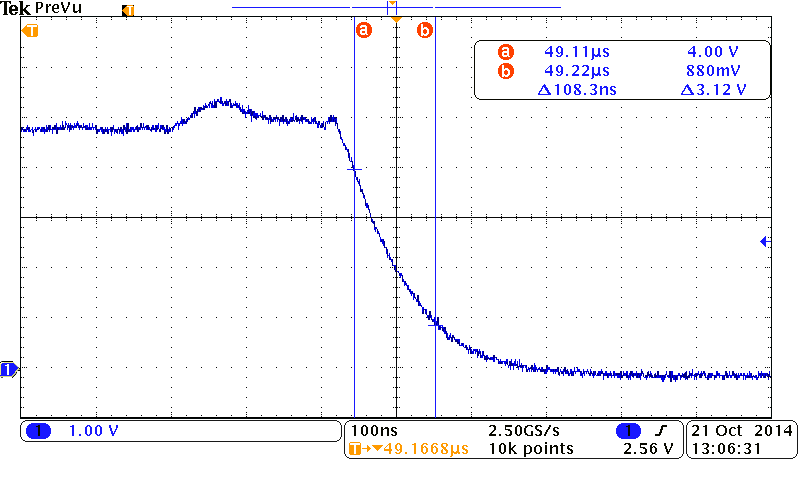


Fig. 1c: The fall time of the output voltage of an inverter with no load

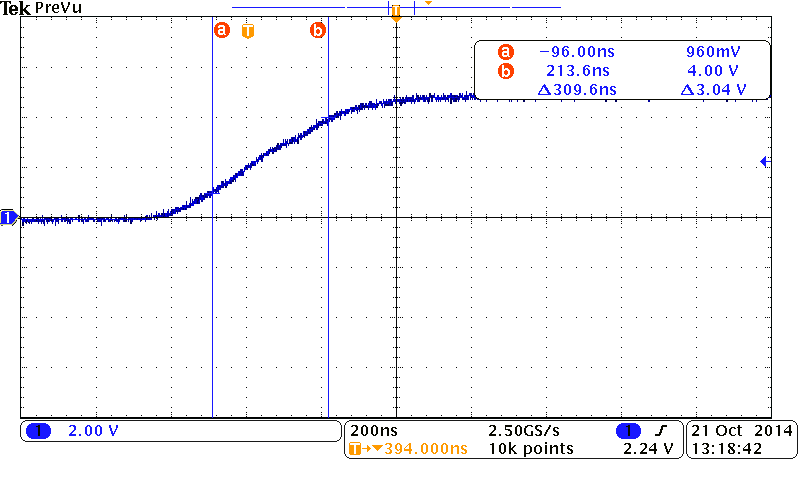


Fig. 2a: The rise time of an inverter's output voltage with 4 inverters connected in parallel to its load.

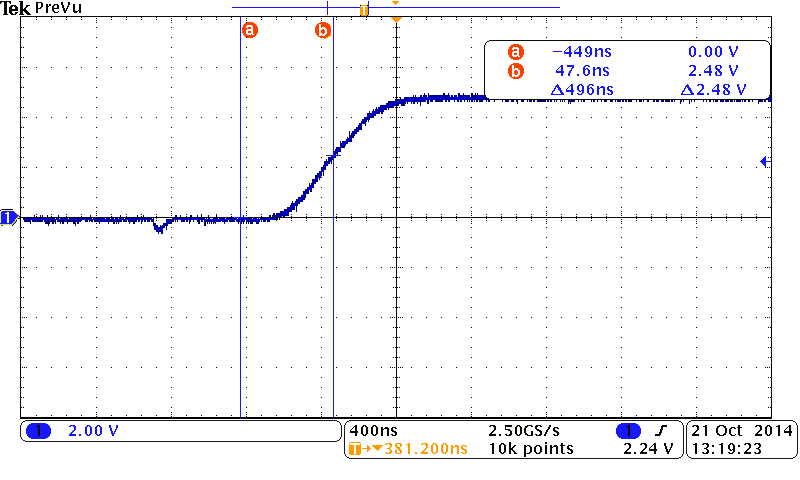
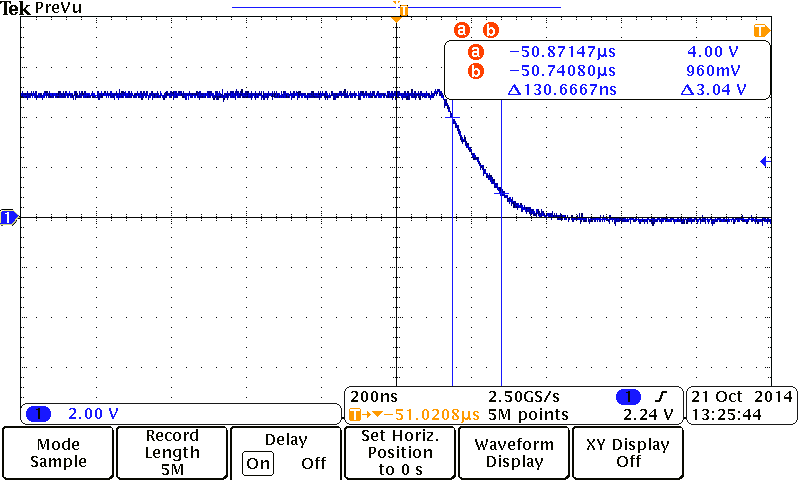


Fig. 2b: The rise time propagation delay with 4 inverters connected.



Fib. 2c: The fall time with 4 inverters connected.

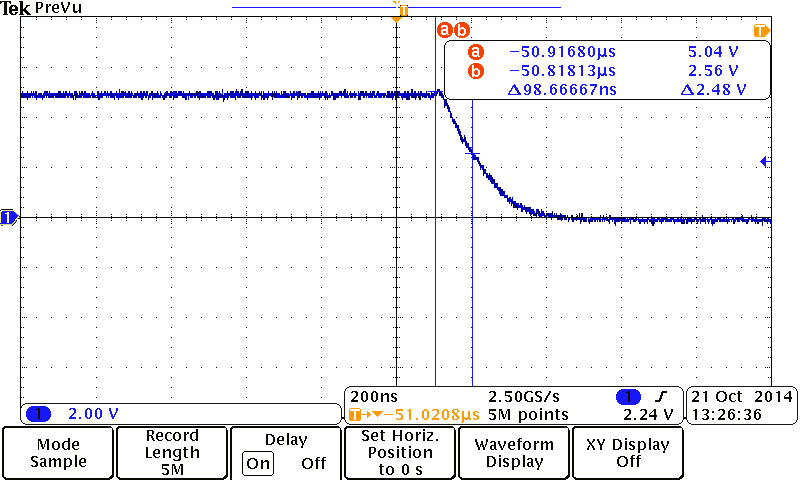


Fig. 2d: The fall time propagation delay with 4 inverters connected.

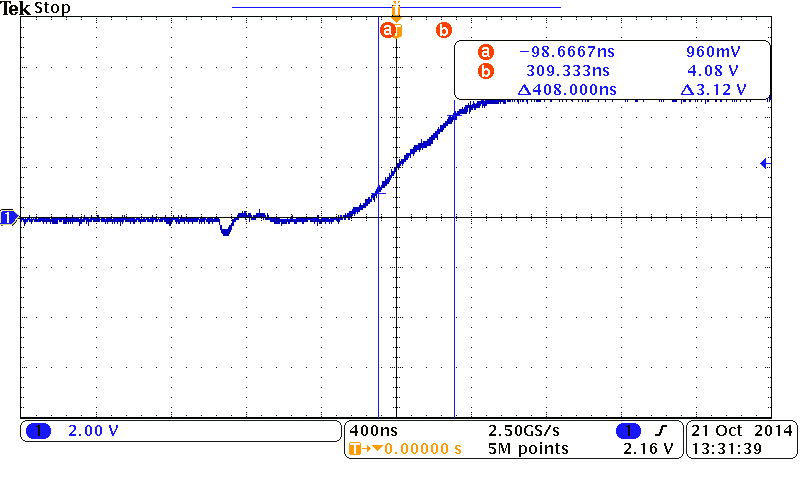


Fig. 3a: The rise time with 8 inverters connected.

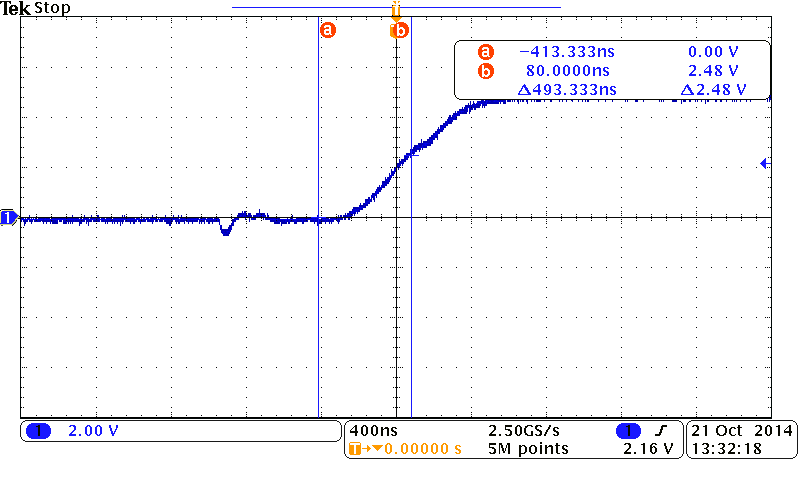


Fig. 3b: The rise time propagation delay with 8 inverters connected.

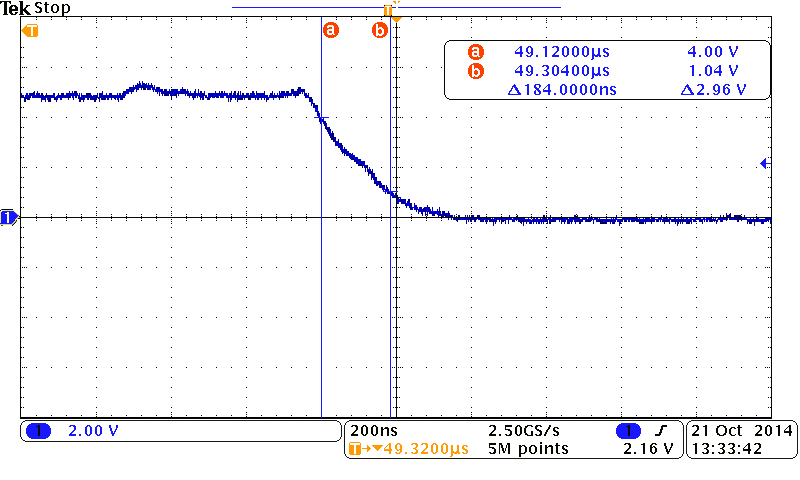


Fig. 3c: The fall time with 8 inverters connected.

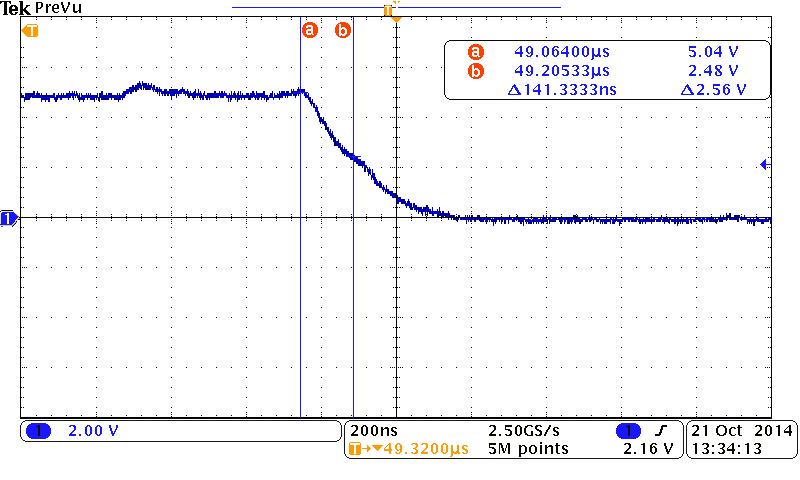


Fig. 3d: The fall time propagation delay with 8 inverters connected.

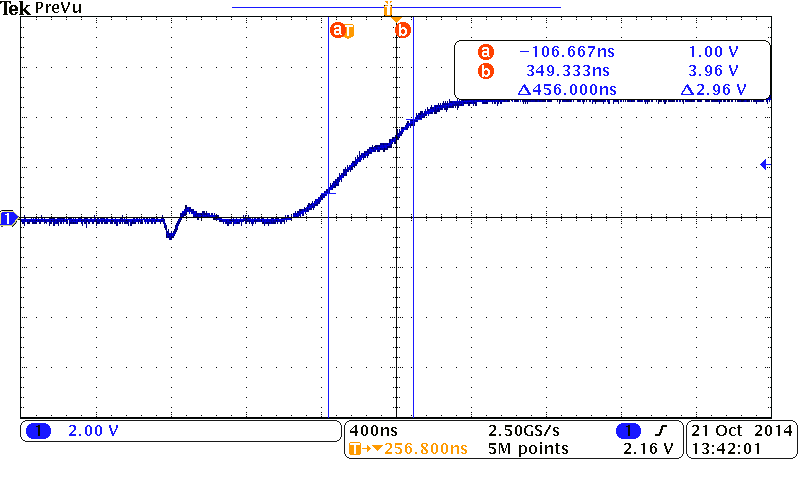


Fig. 4a: The rise time with 12 inverters connected.

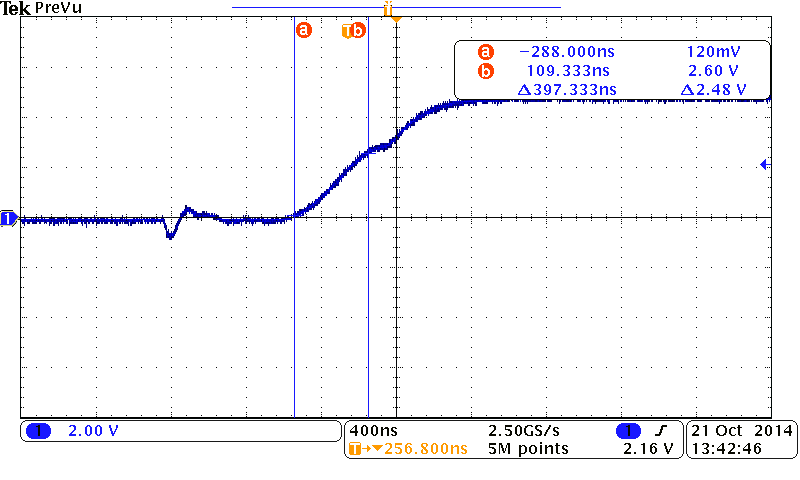


Fig. 4b: The rise time propagation delay with 12 inverters connected.

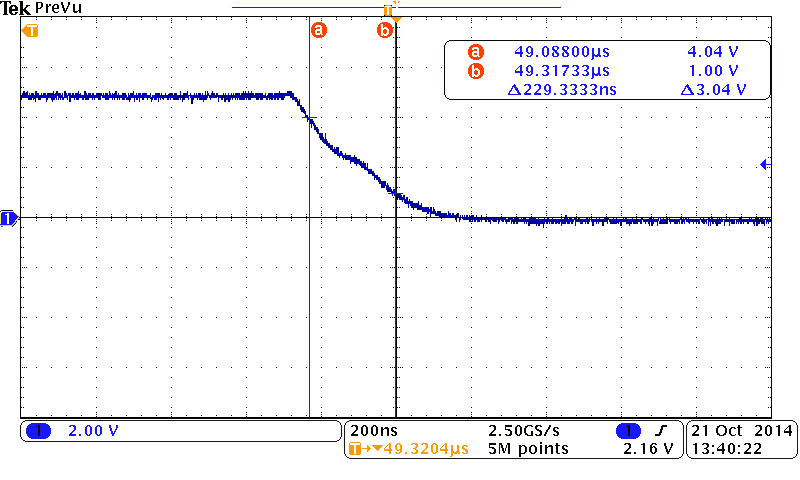


Fig. 4c: The fall time with 12 inverters connected.

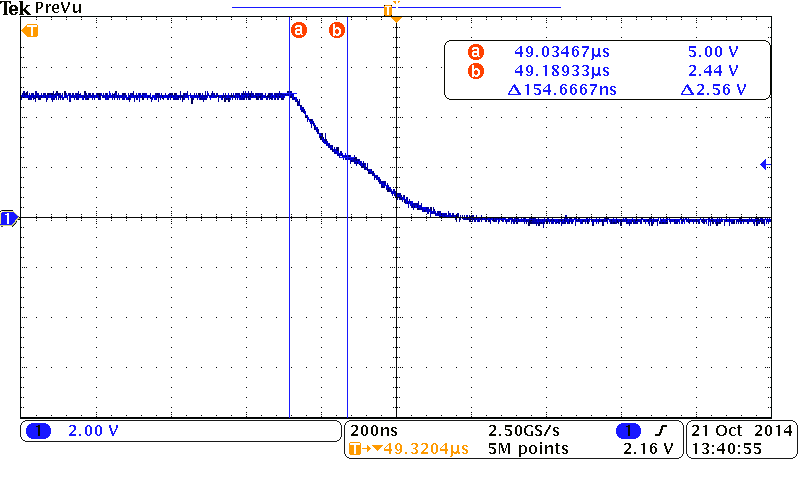


Fig. 4d: The fall time propagation delay with 12 inverters connected.

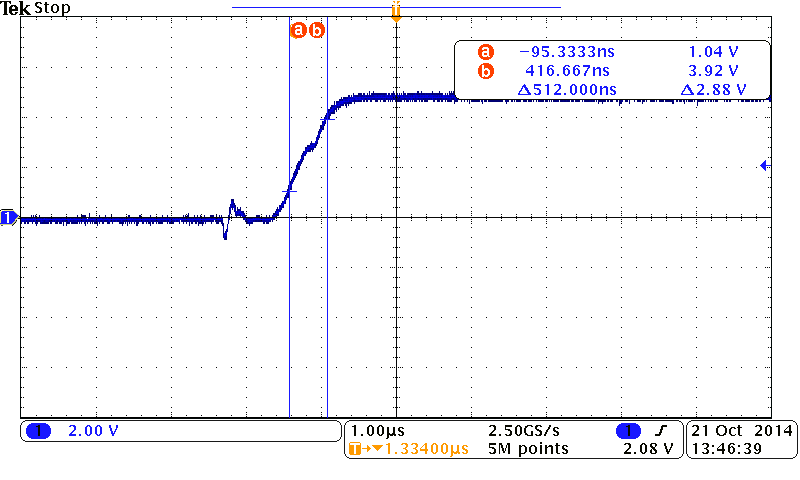


Fig. 5a: The rise time with 16 inverters connected

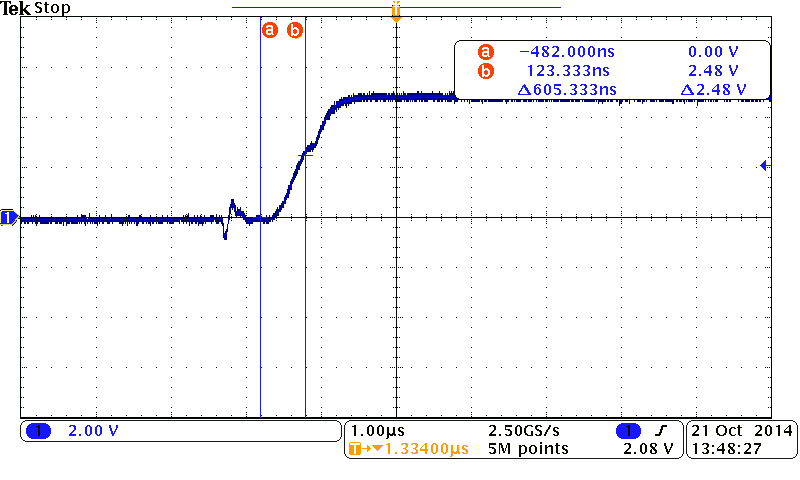


Fig. 5b: The rise time propagation delay with 16 inverters connected

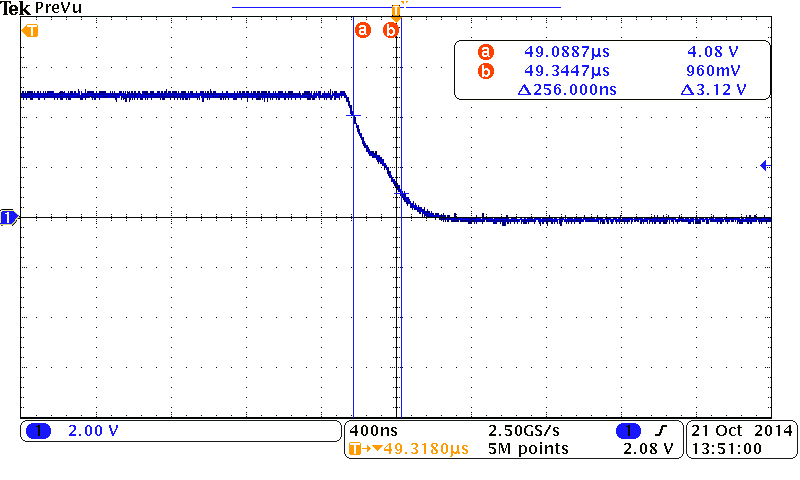


Fig. 5c: The fall time with 16 inverters connected

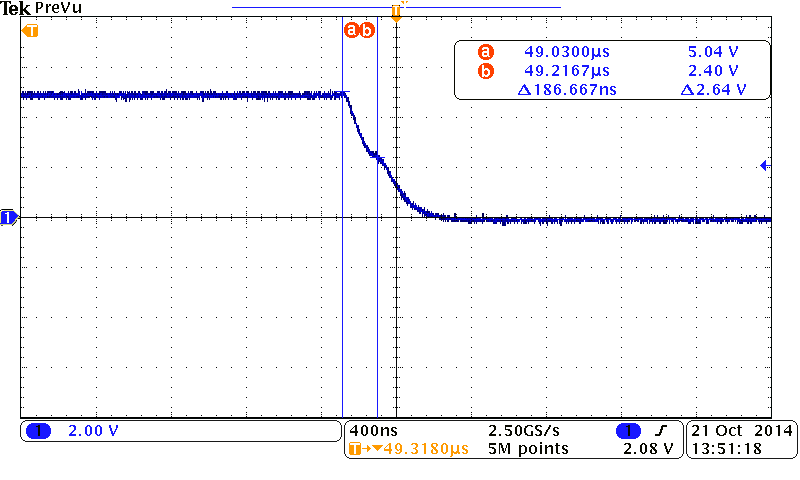


Fig. 5d: The fall time propagation delay with 16 inverters connected

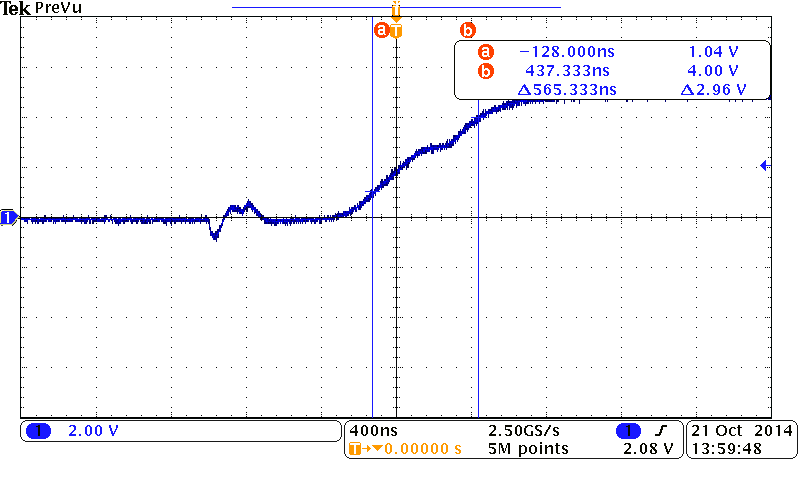


Fig. 6a: The rise time with 20 inverters connected.

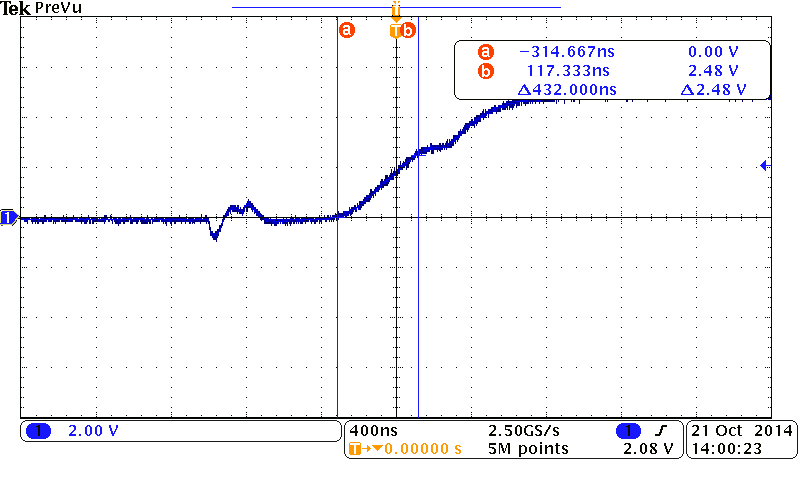


Fig. 6b: The rise time propagation delay with 20 inverters connected

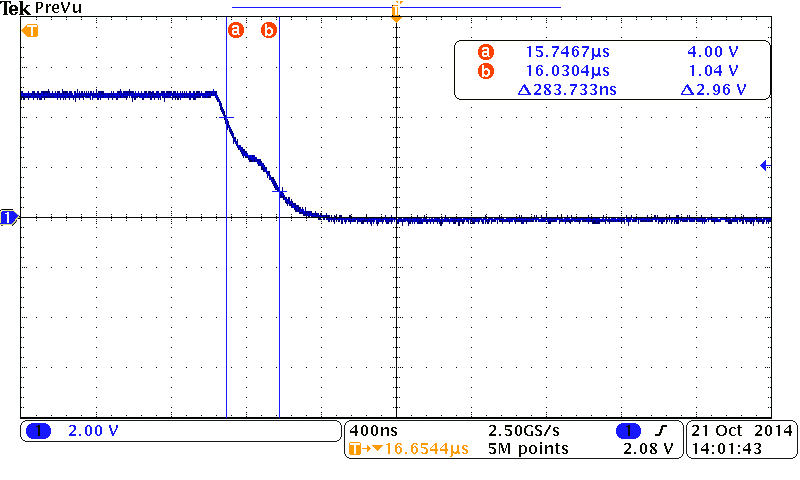


Fig. 6c: The fall time with 20 inverters connected

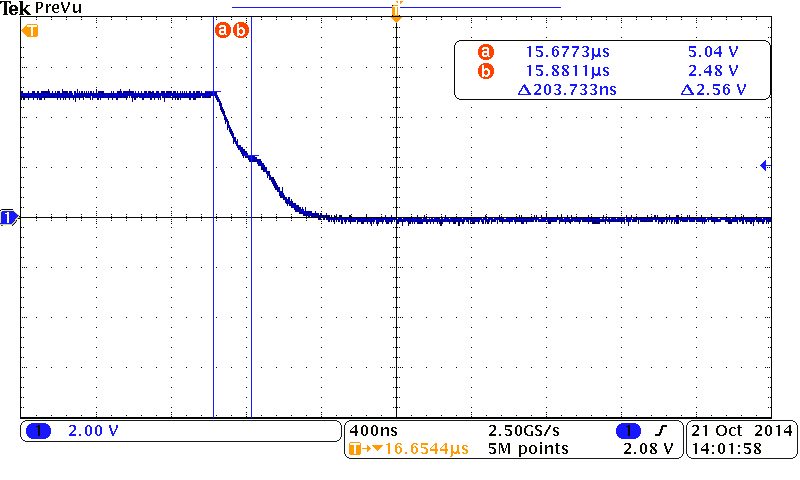


Fig. 6d: The fall time propagation delay with 20 inverters connected.

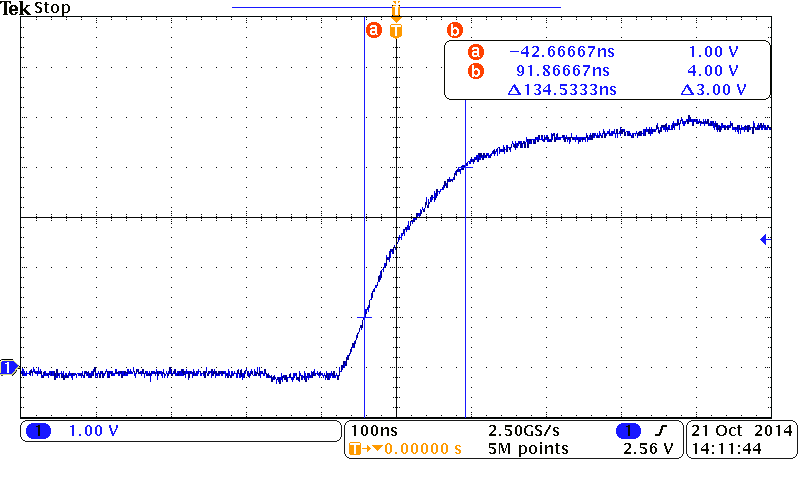


Fig. 7a: The rise time of a CMOS NAND gate with no load.

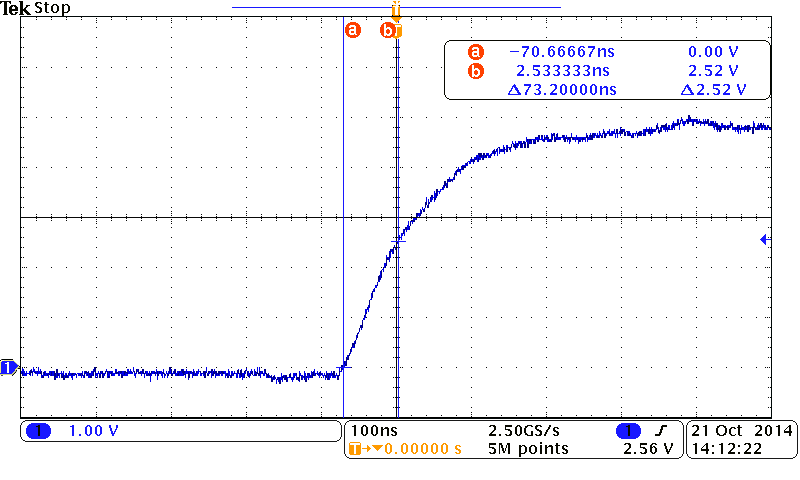


Fig. 7b: The rise time propagation delay of a NAND gate with no load.

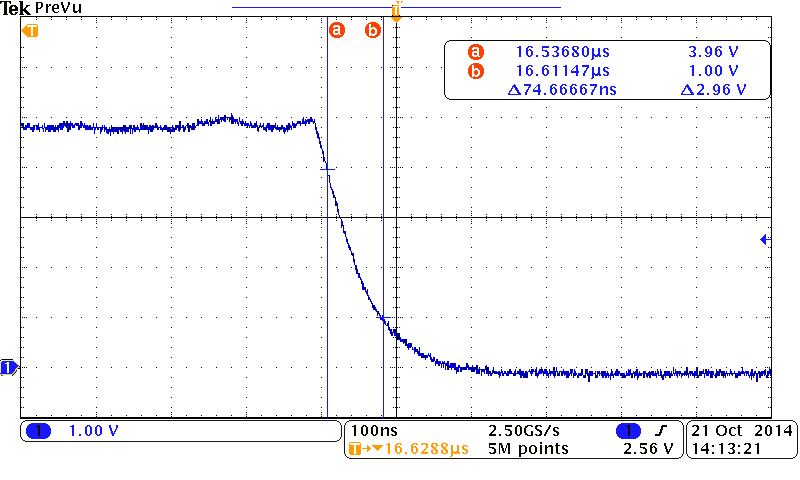


Fig. 7c: The fall time of a NAND gate with no load.

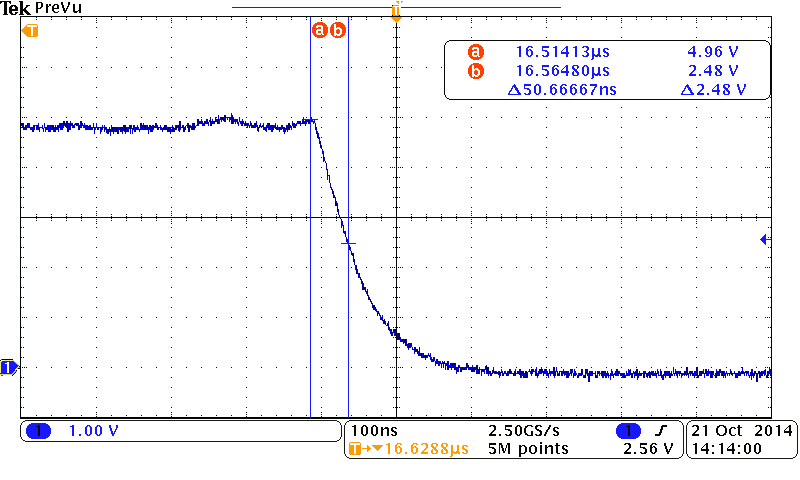


Fig. 7d: The fall time propagation delay of a NAND gate with no load.

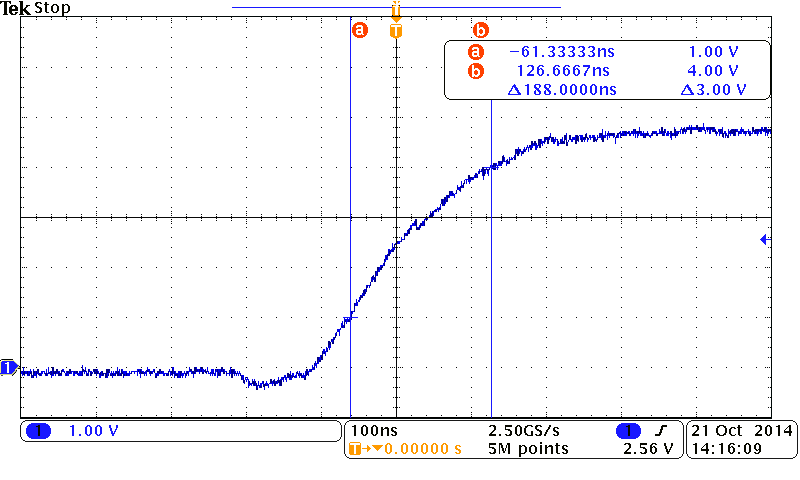


Fig. 8a: The rise time with 4 NAND gates connected.

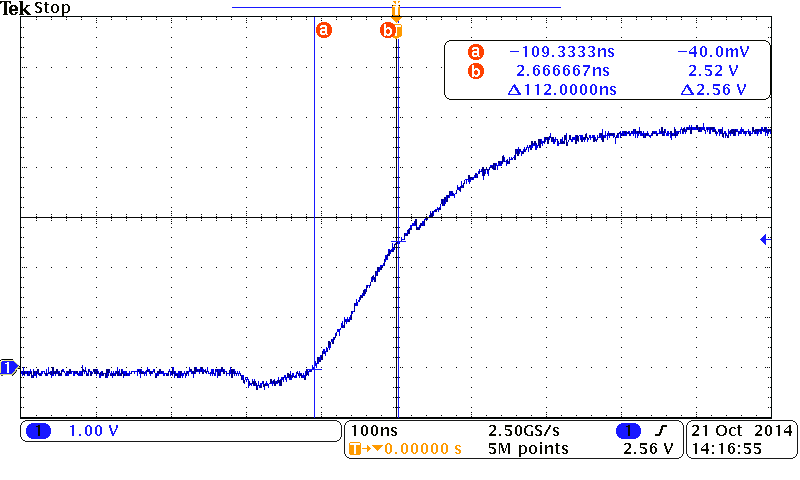


Fig. 8b: The rise delay with 4 NAND gates connected.

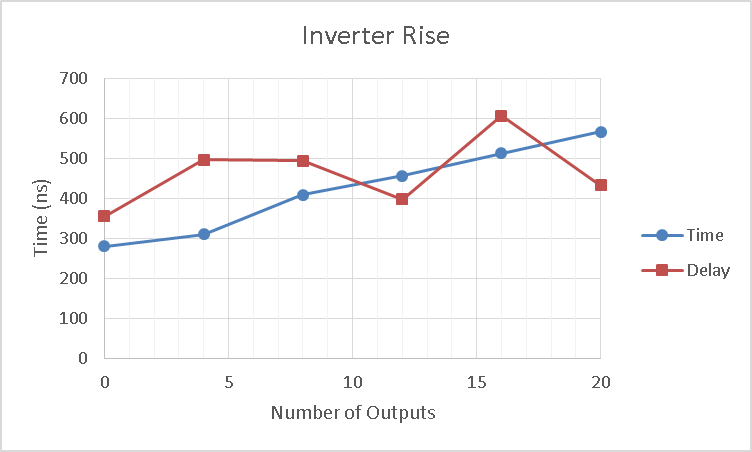


Figure 9a: Test results for inverter rise phase.

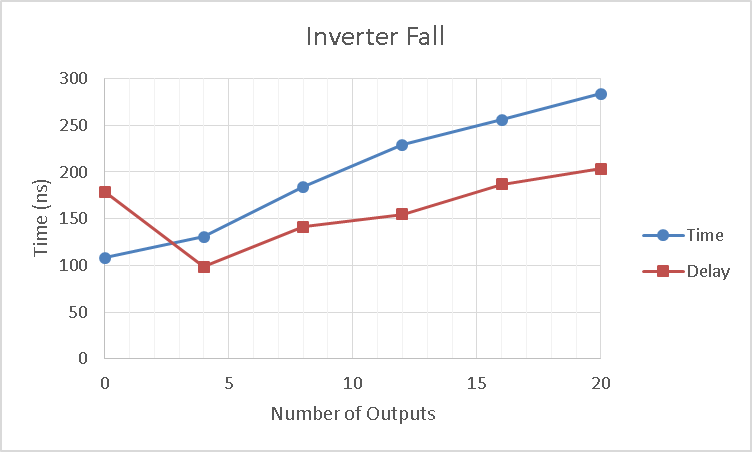


Figure 9b: Test results for inverter fall phase.

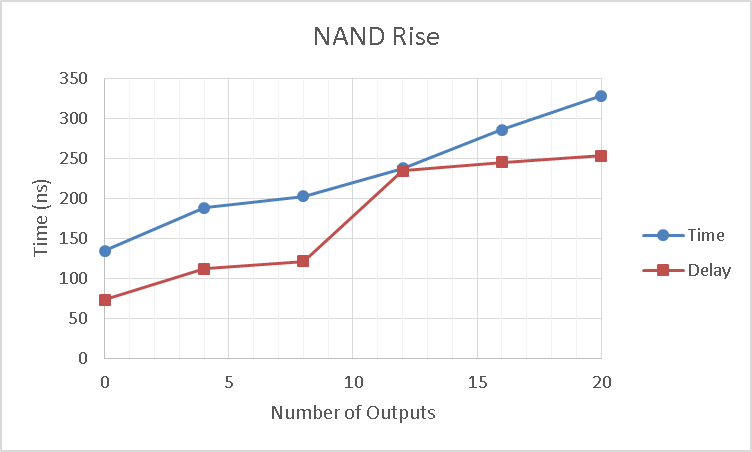


Figure 10a: Test results for NAND rise phase.

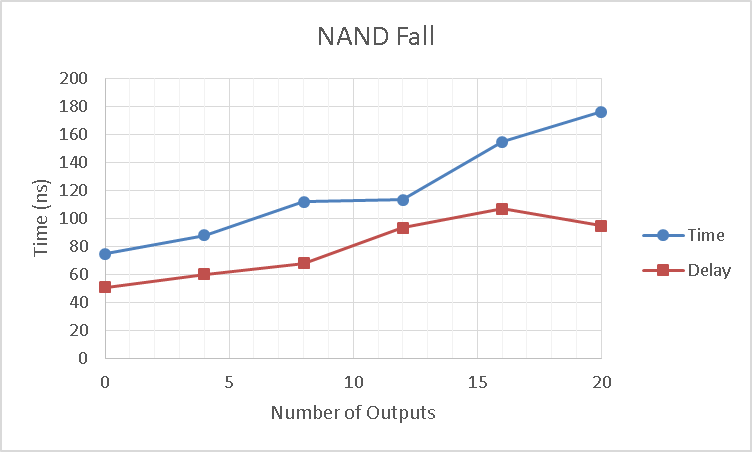


Figure 10b: Test results for NAND fall phase.

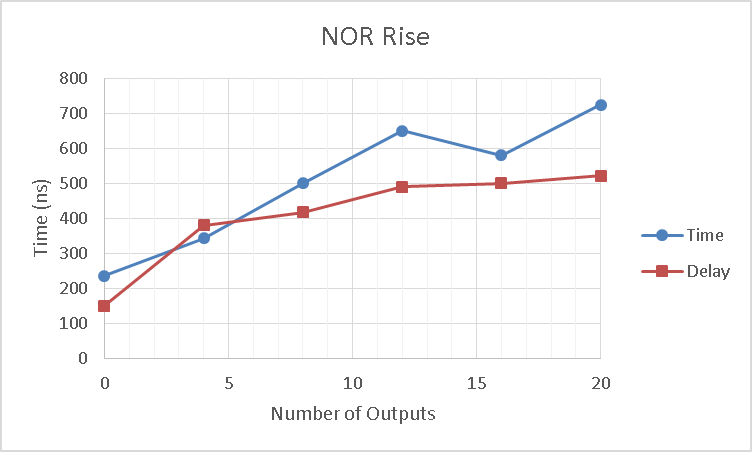


Figure 11a: Test results for NOR rise phase.

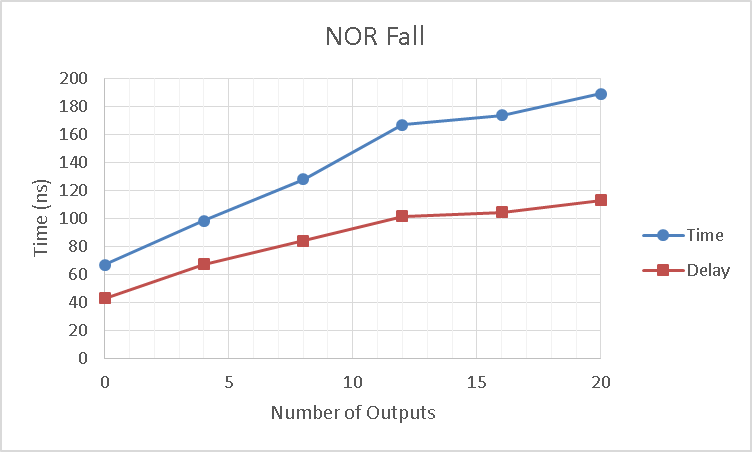


Figure 11b: Test results for NOR fall phase.

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